Claims

[c1] A method of forming at least one field effect transistor having an inverse-T gate structure with at least two ledges extending along a transistor axis from the sides of a central gate structure by a ledge distance, comprising the steps of:

forming a gate dielectric on a portion of a semiconductor substrate having a first polarity;

forming a gate electrode disposed above the gate dielectric and having an inverse-T structure;

implanting a halo implant of said first polarity and a halo concentration in the substrate on opposite sides of the gate electrode, self-aligned to the central gate structure and passing through said ledges to a halo depth;

forming a pair of disposable spacers adjacent to said central gate structure and extending past said ledge distance over a portion of the halo implant;

implanting a self-aligned S/D region of a second polarity opposite said first polarity in the substrate and self-aligned to said disposable spacers, said S/D region having a concentration greater than said halo concentration and having a S/D depth greater than said halo depth;

activating the S/D implant;

implanting in the substrate an extension implant of said second polarity self-aligned to said ledges; and

activating the extension implant.

[c2] A method according to claim 1, in which said step of activating said extension implant is effected by a RTA after the step of activating the S/D.

[c3] A method according to claim 1, in which said disposable spacers are stripped before said step of implanting said extension implant.

[c4] A method according to claim 1, in which said step of implanting said extension implant is effected with an energy such that the implant does not penetrate through the ledges, whereby the halo implant is located beneath the ledges.

[c5] A method according to claim 2, in which said step of implanting said extension implant is effected with an energy such that the implant does not penetrate through the ledges, whereby the halo implant is located beneath the ledges.

[c6] A method according to claim 3, in which said step of implanting said extension implant is effected with an energy such that the implant does not penetrate through the ledges, whereby the halo implant is located beneath the ledges.

[c7] A method according to claim 2, in which said disposable spacers are stripped before said step of implanting said extension implant.

[c8] A method according to claim 7, in which said step of implanting said extension implant is effected with an energy such that the implant does not penetrate through the ledges, whereby the halo implant is located beneath the ledges.

[c9] A method according to claim 1, further comprising the steps of forming a second set of at least one field effect transistor having an inverse-T gate structure with at least two ledges extending along a transistor axis from the sides of a central gate structure by a ledge distance, comprising the steps of:
forming a gate dielectric on a portion of a semiconductor substrate having said second polarity;
forming a gate electrode disposed above the gate dielectric and having an inverse-T structure;
implanting a halo implant of said second polarity and a halo concentration in the substrate on opposite sides of the gate electrode, self-aligned to the central gate structure and passing through said ledges to a halo depth;
forming a pair of disposable spacers adjacent to said central gate structure and extending past said ledge distance over a portion of the halo implant;
implanting a self-aligned S/D region of said first polarity opposite said second polarity in the substrate and self-aligned to said disposable spacers, said S/D region having a concentration greater than said halo concentration and having

a S/D depth greater than said halo depth;

activating the S/D implant;

implanting in the substrate an extension implant of said first polarity self-aligned to said ledges;

activating the extension implant: and connecting the transistors to form a circuit.

[c10] A method of forming a transistor gate electrode having an inverse-T structure with a set of ledges extending along a transistor axis from the sides of a central gate structure by a ledge distance, comprising the steps of:

forming a gate dielectric on a semiconductor substrate having a first polarity;

depositing a ledge layer of a first material over said gate dielectric;

depositing a temporary layer of a second material over said gate dielectric;

forming a first damascene aperture having vertical interior walls and extending down to said ledge layer in said temporary layer;

forming a set of vertical spacers of a third material different from said second material on said interior walls of said damascene aperture, thereby forming a second damascene aperture;

forming a gate electrode disposed above the ledge layer in

said second damascene aperture;

stripping the vertical sidewalls and thereby forming an inverse T gate electrode from the gate electrode and the ledge layer.

[c11] A method according to claim 10, in which said step of stripping said temporary layer is performed after forming the gate and before stripping the sidewalls.

[c12] A method according to claim 10, in which said temporary material is such that it can be removed without damaging the gate electrode; and

said third material is such that it can be removed without damaging the gate electrode.

[c13] A method according to claim 11, further comprising a step of etching that portion of said ledge layer outside said vertical sidewalls after said step of stripping the temporary layer, thereby forming the ledges of said inverse-T gate electrode from said ledge layer.

[c14] A method of forming a transistor gate electrode having an inverse-T structure with a set of ledges extending from the sides of a central gate structure by a ledge distance, comprising the steps of:

forming a gate dielectric on a semiconductor substrate having a first polarity;

depositing a gate layer of a first material over said gate

dielectric;

patterning the gate layer to form a temporary gate structure;

forming an etch-resistant blocking layer having a ledge thickness of a second material over said gate dielectric and over the top surface of the temporary gate structure, leaving vertical walls of the temporary gate structure exposed;

etching the vertical walls of the temporary gate structure with a substantially isotropic etch while the blocking layer blocks the etch from the top surface and from a portion of the temporary gate structure having the same thickness as the ledge thickness, thereby forming the ledges of the inverse-T structure.

[c15] A method according to claim 14, in which said first material is polysilicon and said second material is oxide.

[c16] A method according to claim 1, in which said step of forming a gate electrode comprises the steps of:

forming a gate dielectric on a semiconductor substrate having a first polarity;

depositing a ledge layer of a first material over said gate dielectric;

depositing a temporary layer of a second material over said gate dielectric;

forming a first damascene aperture having vertical interior walls and extending down to said ledge layer in said

temporary layer;

forming a set of vertical spacers of a third material different from said second material on said interior walls of said damascene aperture, thereby forming a second damascene aperture;

forming a gate electrode disposed above the ledge layer in said second damascene aperture;

stripping the vertical sidewalls and thereby forming an inverse T gate electrode from the gate electrode and the ledge layer.

[c17] A method according to claim 16, in which said step of stripping said temporary layer is performed after forming the gate and before stripping the sidewalls.

[c18] A method according to claim 16, in which said temporary material is such that it can be removed without damaging the gate electrode; and

said third material is such that it can be removed without damaging the gate electrode.

[c19] A method according to claim 1, in which said step of forming a gate electrode comprises the steps of:

forming a gate dielectric on a semiconductor substrate having a first polarity;

depositing a gate layer of a first material over said gate dielectric;

patterning the gate layer to form a temporary gate structure;

forming an etch-resistant blocking layer having a ledge thickness of a second material over said gate dielectric and over the top surface of the temporary gate structure, leaving vertical walls of the temporary gate structure exposed;

etching the vertical walls of the temporary gate structure with a substantially isotropic etch while the blocking layer blocks the etch from the top surface and from a portion of the temporary gate structure having the same thickness as the ledge thickness, thereby forming the ledges of the inverse-T structure.

[c20] A method according to claim 19, in which said first material is polysilicon and said second material is oxide.